

Function Description

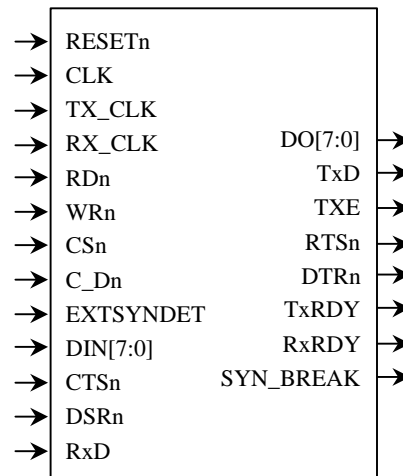
The C8251 programmable communications interface (USART) megafunction provides data formatting and control to a serial communication channel.

The megafunction has select, read/write, interrupt and bus interface logic features that allow data transfers over an 8-bit bi-directional parallel data bus system. With proper formatting and error checking, the megafunction can transmit and receive serial data, supporting both synchronous and asynchronous operation.

Features

- ◆ Synchronous and asynchronous operation
- ◆ Programmable data word length, parity and stop bits
- ◆ Parity, overrun and framing error checking instructions and counting loop interactions
- ◆ Supports up to 1.750 Mbps transmission rates
- ◆ Divide-by 1,-16,-64 mode
- ◆ False start bit deletion
- ◆ Automatic break detection
- ◆ Internal and external synch character detection
- ◆ Peripheral modem control functions
- ◆ The C8251 was developed in VHDL and synthesizes to approximately 2,300 gates depending on the technology used
- ◆ Functionality based on the Intel 8251A device

Symbol



Pin Description (Continuation)

Name	Type	Polarity	Description
D0[7:0]	Out	-	Data Output Bus
TxD	Out	-	Transmit Data
TxE	Out	Low	Transmitter empty
RTSn	Out	Low	Request-to-Send
DTRn	Out	Low	Data Terminal Ready
TxRDY	Out	High	Transmit ready
RxRDY	Out	High	Receiver ready
SYN_BREAK	Out	Low	Sync/Break detect

Applications

- Serial data communications applications
- Modem interface

Functional Description

The C8251 core is partitioned into modules as shown in figure 1 and described below.

Block1

The Receiver Buffer and Control accept serial data, convert it to parallel format, check for parity, framing, overrun, break and send the formatted data to the CPU.

Block2

The Transmitter Buffer and Control logic accept parallel data from the Data Bus Buffer, convert it to serial, inserting required characters or bits depending on communication protocol, and output the formatted serial stream to the TxD output pin.

Block3

The Modem Control Logic consists of a set of inputs and outputs that can be used to interface to almost any modem .

Block4

The CPU interface shares common interface signals with the CPU: Data Bus, Read, Write, Chip selects, Reset and Master CLK.

Core Assumptions

- Active-low reset input
- The 1½ stop bit mode is not supported
- Separate EXTSYNDET and SYN_BREAK signals
- The bi-directional data bus has been split in two separate data buses: DIN and DO

Verification Methods

The C8251 USART megafunction's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model which contained the original Intel 8251 chip, and the results compared with the megafunction's simulation outputs.

Device Utilization & Performance

Target Device	Speed Grade	Utilization		Performance F_{max}	Availability
		LCs	EABs		
EPF6010A	-1	533	-	19 MHz	Now
EPF8820A	-2	533	-	12 MHz	Now
EPF10K10	-3	533	-	16 MHz	Now
EPF10K10A	-1	533	-	25 MHz	Now

Deliverables

Encrypted Licenses

- Post-synthesis AHDL
- Assignment & Configuration
- Symbol file
- Include file
- Graphic Design file of test circuit
- Vectors for testing the functionality of the megafunction

VHDL Source Licenses

- VHDL RTL source code
- Testbench
- Example testbench wrapper for post-route simulation
- Vectors for testbench
- Simulation script
- Synthesis script
- Expected results for testbench

Megafunction Modifications

The C8251 megafunction can be customized to include:

- 16 bit Internal Baud Rate Generator
- Remove either synchronous or asynchronous sections in order to reduce area

Please contact CAST directly for any required modifications.

CAST, Inc.

24 White Birch Drive

Pomona, New York 10907 USA

Phone: +1 914-354-4945 Fax: +1 914-354-0325

E-Mail: info@cast-inc.com URL: www.cast-inc.com

The C8251 megafunction is licensed from Moxsyn S.r.l.