



C16550 Universal Asynchronous Receiver/Transmitter with FIFOs

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Product Specification



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Features

- Capable of running with all existing 16450 and 16550A Software
- Asynchronous operation
- In FIFO mode, Transmitter and Receiver are each buffered with 16-byte FIFOs to reduce the number of interrupts of the CPU
- Programmable data word length (5 - 8 bit), parity and stop bits
- Parity, overrun and framing error checking
- Programmable Baud Rate Generator allows division of any reference clock by 1 to $(2^{16}-1)$ and generates an internal 16 X Clock
- False start bit detection
- Automatic break generation and detection
- Internal diagnostic capabilities
- Peripheral modem control functions

Table 1: Core Implementation Data

Supported Family	Device Tested	CLB Slices ²	Clock IOBs	IOBs ¹	Performance (MHz)	Xilinx Tools	Special Features
Virtex	V50-6	580	4	39	53	M2.1i	None
Virtex-E	V50E-8	580	4	39	68	M2.1i	None
Spartan-II	2S50-6	580	4	39	51	M2.1i	None

Notes:

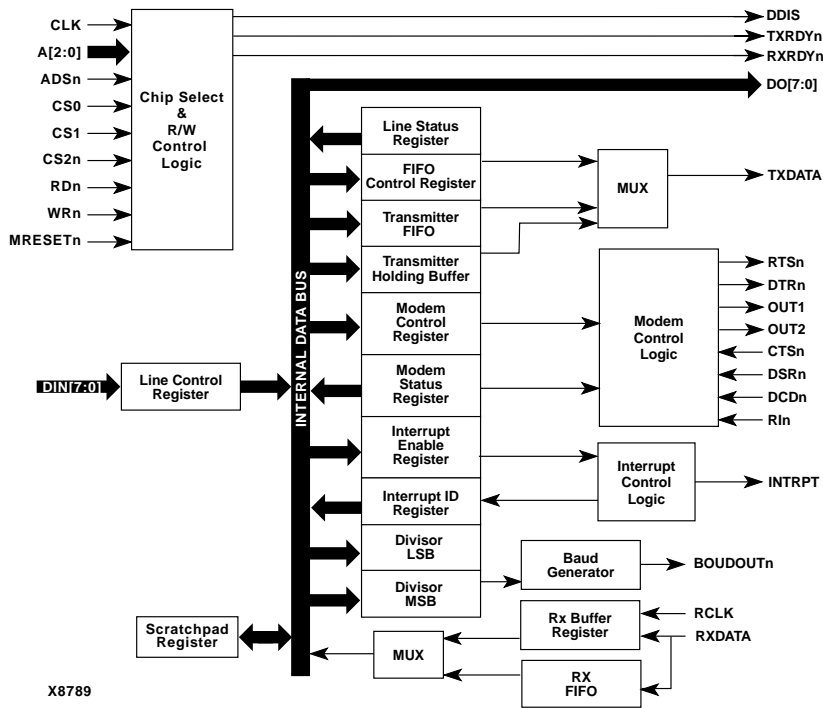
1. Assuming all core I/Os are routed off-chip.

2. Optimized for speed.

AllianceCORE™ Facts	
Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core design document
Design File Formats	EDIF, .ngo, .XNF Netlist; VHDL Source RTL available extra
Constraints File	C16550.ucf
Verification	VHDL testbench, test vectors
Instantiation Templates	VHDL, Verilog
Reference designs & application notes	None
Additional Items	None
Simulation Tool Used	
1076-compliant VHDL simulator Verilog simulator	
Support	
Support provided by CAST, Inc.	

Applications

The C16550 core is used in serial data communications and modem applications.



X8789

Figure 1: C16550 Asynchronous Receiver/Transmitter with FIFOs Block Diagram

General Description

The C16550 programmable asynchronous communications interface (UART) megafunction provides data formatting and control to a serial communication channel.

The megafunction has select, read/write, interrupt and bus interface logic features that allow data transfers over an 8-bit bi-directional parallel data bus system. With proper formatting and error checking, the megafunction can transmit and receive serial data, supporting asynchronous operation.

Functional Description

The C16550 core is partitioned into modules as shown in Figure 1 and described below.

Chip Select & R/W Control Logic

The chip select and R/W control logic controls the internal chip addressing.

Line Control Register (LCR)

The Line Control Register is used to specify the data communication format. The break feature, parity, stop bits and word length can be changed by writing to the appropriate bits in LSR.

Line Status Register (LSR)

This register provides information on the status of data transfers between the C16550 and the CPU.

Interrupt Enable Register (IER)

The Interrupt Enable Register masks interrupts from the modem status registers, line status, transmitter empty and receiver ready to the INTRPT output pin.

Modem Status Register (MSR)

This register provides the current state of modem control lines.

Modem Control (Register & Logic)

This register controls the interface lines with the MODEM (MODEM control logic) and changes the status of the C16550 from normal operating mode and local loop-back mode (diagnostics mode).

Transmitter Holding Buffer

The transmitter section is composed of a Transmit Holding Register (THR) and a Transmit Shift Register (TSR). Writing to THR will transfer the contents of the data bus (DIN 7-0) to the Transmit Holding Register every time that the THR

or TSR is empty. This write operation should be done when Transmit Holding Register Empty (THRE) is set.

Receiver Buffer & RX FIFO

This register contains the assembled received data. On the falling edge of the start bit, the receiver section starts its operations. The start bit is valid if the RXDATA is still low at the middle sample of Start bit, thus preventing the receiver from assembling a false data character.

The receiver buffer is actually a 16-byte FIFO.

Scratchpad Register (SR)

This register stores the temporary byte for variable use.

FIFO Control Register (FCR)

This register is used to control FIFOs' logic (to enable, to clear, to set FIFOs' trigger level and set the type of DMA signaling).

Interrupt Identification Register (IIR)

The Interrupt Identification Register provides the source of interrupt among four levels of prioritized interrupt conditions in order to minimize the CPU overhead during data transfers.

Interrupt Control Logic

The C16550 contains an interrupt generation and prioritization logic. When an interrupt is generated the IIR indicates that an interrupt is pending and also the type of interrupt between various available. The C16550 provides four prioritized levels of interrupt:

- Priority 1 Receiver line status (highest priority)
- Priority 2 Receiver data ready or receiver character timeout
- Priority 3 Transmitter holding register empty
- Priority 4 Modem Status (lowest priority)

Baud Generator & LSB and MSB Divisor Registers

The C16550 contains a programmable baud rate generator that takes any clock input from DC-20MHz and dividing it by any divisor from 1 to $(2^{16} - 1)$. The output frequency of the Boudoutn is equal to 16X of the transmission baud rate. The two registers divisor MSB and divisor LSB are used to store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization in order to ensure desired operation of the baud generator.

The formula for the divisor is:

$$\text{divisor} = \text{CLKIN frequency in } \div (\text{desired baud rate} \times 16)$$

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
CLK	Input	Master Clock; uses 1 global IOB pin
A[2:0]	Input	Register Select
ADSn	Input	Address Strobe
CS0	Input	Chip Select 0
CS1	Input	Chip Select 1
CS2n	Input	Chip Select 2
RDn	Input	Read Control; uses 1 global IOB pin
WRn	Input	Write Control; uses 1 global IOB pin
MRESETn	Input	External Reset
DIN[7:0]	Input	Data Input Bus
DDIS	Output	Driver Disable
CSOUT	Output	Chip Select Out
TxRDYn	Output	Transmit ready
RxRDYn	Output	Receiver ready
D0[7:0]	Output	Data Output Bus
TXDATA	Output	Transmit Data
RTSn	Output	Request-to-Send
DTRn	Output	Data Terminal Ready
OUT1	Output	Output 1
OUT2	Output	Output 2
CTSn	Input	Clear-to-Send
DSRn	Input	Data Set Ready
DCDn	Input	Data Carrier Detect
RIn	Input	Ring Indicator
INTRPT	Output	Interrupt
BOUDOUT	Output	Baud Out
RCLK	Input	Receive Clock; uses 1 global IOB pin
RXDATA	Input	Receive Data

Core Modifications

The C16550 core can be customized to include:

- Different FIFOs size (separately for Transmitter and Receiver)
- Removal of internal baud rate generator
- Different CPU interface

Please contact CAST directly for any required modifications.

Pinout

The pinout of the C16550 core has not been fixed to specific FPGA I/O, allowing flexibility with a users application. Signal names are shown in the block diagram in Figure 1 and described in Table 2.

Core Assumptions

- The bi-directional data bus has been split into two separate buses: DIN[7:0] and DO[7:0]
- The 1.5 stop bit mode (for 5 bit word length) is not supported
- Signals rd2, wr2, xin and xout have been eliminated from the interface

Verification Methods

The C16550 UART core's functionality has been extensively tested with a VHDL testbench and a large number of test patterns.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

This product is available from the AllianceCORE[®] partner listed on the first page. Please contact the partner for pricing and more information.

The C16550 core is licensed from Moxsyn S.R.L.

Related Information

Data Transmission Circuits 1993 Data Book

Contact:

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