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Features

- Full double buffering
- Asynchronous operation
- Independently controlled Transmit, Line Status, Receive, and Data Set Interrupts
- Programmable data word length (5 - 8 bit), parity and stop bits
- Parity, overrun and framing error checking
- Supports up to 1.5 Mbps transmission rates
- Programmable Baud Rate Generator allows division of any reference clock by 1 to $(2^{16}-1)$ and generates an internal 16 X Clock
- False start bit detection
- Automatic break generation and detection
- Internal diagnostic capabilities
- Peripheral modem control functions

AllianceCore™ Facts	
Core Specifics	
See Table 1	
Provided with Core	
Documentation	Core documentation
Design File Formats	.ngo, EDIF Netlist, or VHDL Source RTL
Constraints File	NCF
Verification Tool	VHDL
Schematic Symbols	None
Evaluation Model	None
Reference designs & Application notes	None
Additional Items	None
Design Tool Requirements	
Xilinx Core Tools	M2.1i
Entry/Verification Tool	VHDL RTL
Support	
Support provided by CAST, Inc.	

Table 1: Core Implementation Table

FPGA	Slices ²	Global IOBs	IOBs ¹	Performance (MHz)	Speed Grade
Spartan-II	225	1	40	60	-6
Virtex	225	1	40	66	-6
Virtex-E	225	1	40	77	-8

Notes:

1. Assuming all core I/O is routed off-chip.
2. Optimized for speed

Applications

The C8250 core is used in serial data communications and modem applications.

General Description

The C8250 programmable communications interface (UART) core provides data formatting and control to a serial communication channel.

The core has select, read/write, interrupt and bus interface logic features that allow data transfers over an 8-bit bi-directional parallel data bus system. With proper formatting and error checking, the core can transmit and receive serial data, supporting both synchronous and asynchronous operation.

Functional Description

The C8250 core is partitioned into modules as shown in figure 1 and described below.

Chip Select & R/W Control Logic

The chip select and R/W control logic controls the internal chip addressing .

Line Control (LCR)

The Line Control Register is used to specify the data communication format. The break feature, parity, stop bits and word length can be changed by writing to the appropriate bits in LSR.

Line Status (LSR)

This register provides information on the status of data transfers between the C8250 and the CPU.

Interrupt Enable (IER)

The Interrupt Enable Register masks interrupts from the modem status registers, line status, transmitter empty and receiver ready to the INTRPT output pin.

Modem Status (MSR)

This register provides the current state of modem control lines.

Modem Control (Register & Logic)

This register controls the interface lines with the MODEM (MODEM control logic) and changes the status of the C8250 from normal operating mode and local loop-back mode (diagnostics mode).

Transmitter Holding Buffer

The transmitter section is composed of a Transmit Holding Register (THR) and a Transmit Shift Register (TSR). Writing to THR will transfer the contents of the data bus (DIN 7-0) to the Transmit Holding Register every time that the THR or TSR is empty. This write operation should be done when Transmit Holding Register Empty (THRE) is set.

Receiver Buffer

This register contains the assembled received data. On the falling edge of the start bit, the receiver section starts its operations. The start bit is valid if the RXDATA is still low at the middle sample of Start bit, thus preventing the receiver from assembling a false data character.

Interrupt Identification (IIR)

The Interrupt Identification Register provides the source of interrupt among four levels of prioritized interrupt conditions in order to minimize the CPU overhead during data transfers.

Interrupt Control Logic

The C8250 contains an interrupt generation and prioritization logic. When an interrupt is generated the IIR indicates that an interrupt is pending and also the type of interrupt between various available.

The C8250 provides four prioritized levels of interrupt:

Priority 1 - Receiver line status (highest priority)

Priority 2 - Receiver data ready or receiver character timeout

Priority 3 - Transmitter holding register empty

Priority 4 - Modem Status (lowest priority)

Scratchpad (SR)

This register stores the temporary byte for variable use.

Baud Generator & LSB and MSB Divisor Registers

The C8250 contains a programmable baud rate generator that takes any clock input from DC-20MHz and dividing it by any divisor from 1 to $(2^{16} - 1)$. The output frequency of the Baudoutn is equal to 16X of the transmission baud rate. The two registers **divisor MSB** and **divisor LSB** are used to store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization in order to ensure desired operation of the baud generator.

The formula for the divisor is:

$$\text{divisor} = \text{CLKIN frequency in } \div (\text{desired baud rate} \times 16)$$

Core Modifications

The C8250 core can be customized to include:

- Removal of internal baud rate generator
- Different CPU interface

Please contact CAST directly for any required modifications.

Pinout

The pinout of the C8250 core has not been fixed to specific FPGA I/O, allowing flexibility with a users application. Signal names are shown in the block diagram in Figure 1, and in Table 2.

Table 2. Core Signal Pinout

Signal	Signal Direction	Description
RESET	In	External reset
CLK	In	Master clock
RCLK	In	Receive clock
ADSn	In	Address strobe
RDn	In	Read control
WRn	In	Write control
CS0	In	Chip Select 0
CS1	In	Chip Select 1
CS2n	In	Chip Select 2
DIN[7:0]	In	Data Input Bus
CTSn	In	Clear-to -Send
DSRn	In	Data Set Ready
DCDn	In	Data Carrier Detect
RXDATA	In	Receive Data
Rin	In	Ring Indicator
A[2:0]	In	Register Select
DO[7:0]	Out	Data Output Bus
TXDATA	Out	Transmit Data
DDIS	Out	Driver Disable
RTSn	Out	Request-to-Send
DTRn	Out	Data Terminal Ready
OUT1n	Out	Output 1
OUT1n	Out	Output 2
INTRPT	Out	Interrupt
BAUDOUTn	Out	Baud Out

Core Assumptions

- The bi-directional data bus has been split into two separate buses: DIN[7:0] and DO[7:0]
- The 1½ stop bit mode (for 5 bit word length) is not supported
- Signals rd2, wr2, xin, xout and csout have been eliminated from the interface

Verification Methods

The C8250 UART core's functionality has been extensively tested with a VHDL testbench and a large number of test patterns.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

This product is available from the CAST, Inc. Please contact CAST for pricing and more information.

The C8250 core is licensed from Moxsyn S.r.l.

Related Information

Data Transmission Circuits 1993 Data Book

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